Apollo VPX PCIset

EP-5BVPXB

ISA PCI MainBoard

with Onboard PCI IDE and Super Multi-I/O.

TRADEMARK

The specification is subject to change without notice.

V113

Package Checklist

Please check your package which should include all items listed below. If you find any item damaged or any missing item, please contact your supplier.

- One motherboard
- One manual
- One parallel port ribbon cable
- Two serial port ribbon cables
- One IDE ribbon cable
- One floppy ribbon cable
- One optional PS/2 mouse cable

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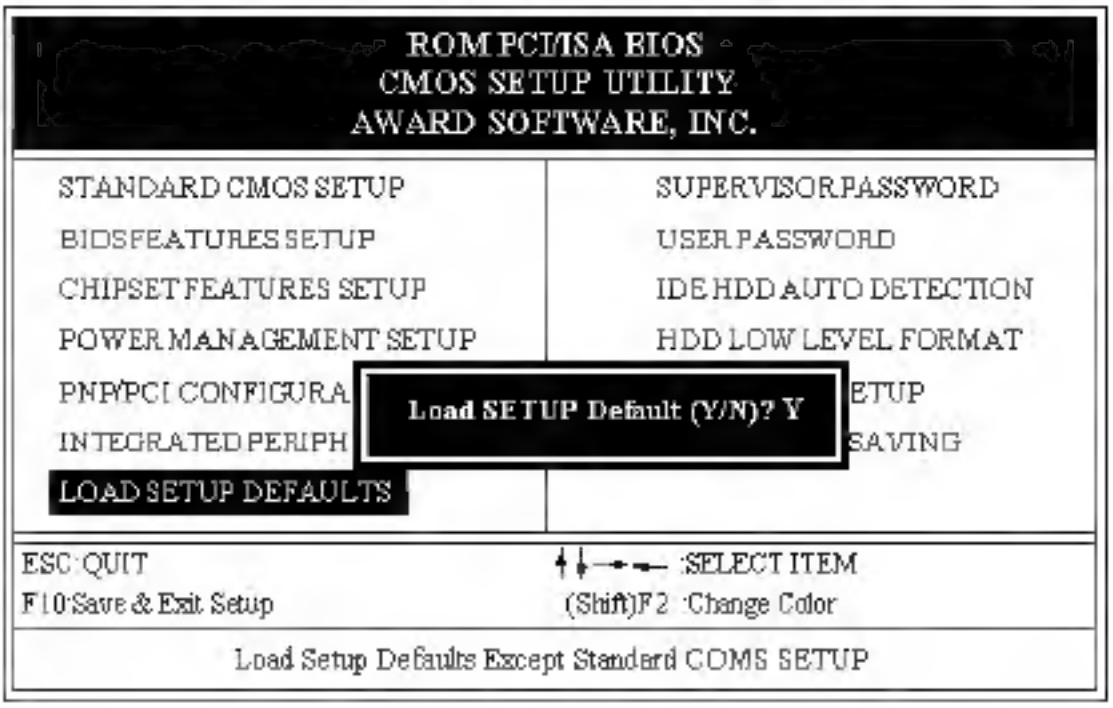
NOTE :

The "**LOAD SETUP DEFAULTS**" function loads the system default data directly from ROM and initializes the associated hardware properly. This function is necessary when you accept this mainboard, or the system CMOS data will corrupt.



LOAD SETUP DEFAULT

Chapter 1
Introduction

The 5BVPXB mainboard is a high performance system hardware based on Intel Pentium® processor and is equipped with four PCI slots, three standard ISA slots, Super Multi-I/O controller and dual port PCI-IDE connectors for the future expansion. The hardware dimension is 220mm x 210mm with a four-layer-design technology.

Specification

- VIA Apollo VPX/97 PCIset chipset.
- Intel **Pentium®** Processor, AMD K5/K6 & Cyrix 6x86/6x86L/6x86MX operating at **90 ~ 333 MHz** and **P55C** with **321 ZIF socket 7** and scalability to accept faster Processors in the future.
- Supports up to 192 MegaBytes of DRAM (a minimum of 8 MB) on board (72-pin SIMM x 2 & 168-pin DIMM x 1). BIOS will autometically detect and configure FP/EDO and Synchronous DRAM (Refer to Chapter 2-3 System Memory Configuration)
- Supports 512KB Onboard Pipelined Burst (synchronous) L2 **Write Back/ Through Cache.**
- Supports three 16 bit ISA slots and four 32 bit PCI slots and provides two independent high performance PCI IDE interfaces capable of supporting **PIO Mode 3/4 and Ultra-DMA33** devices. The **5BVPXB** supports four PCI Bus Masters and a jumperless PCI INT# control scheme which reduces configuration confusion when plugging in PCI I/O controller card(s).
- Supports **ATAPI** (e.g. **CD-ROM**) devices on both IDE interfaces.
- Supports 1 floppy port, 1 parallel port (EPP,ECP port), 2 serial ports (16550 Fast UART compatible) and 1 USB Connector.
- Supports a **PS/2** style mouse and standard AT style keyboard connectors.
- Supports Award Plug & Play BIOS. The BIOS is stored in Flash EPROM form. It provides better upgradeability for the system.
- Supports CPU Hardware sleep and SMM (System Management Mode).
- **5BVPXB** utilizes Lithium battery which provides environmental protection and longer battery life.

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5BVPXB Layout

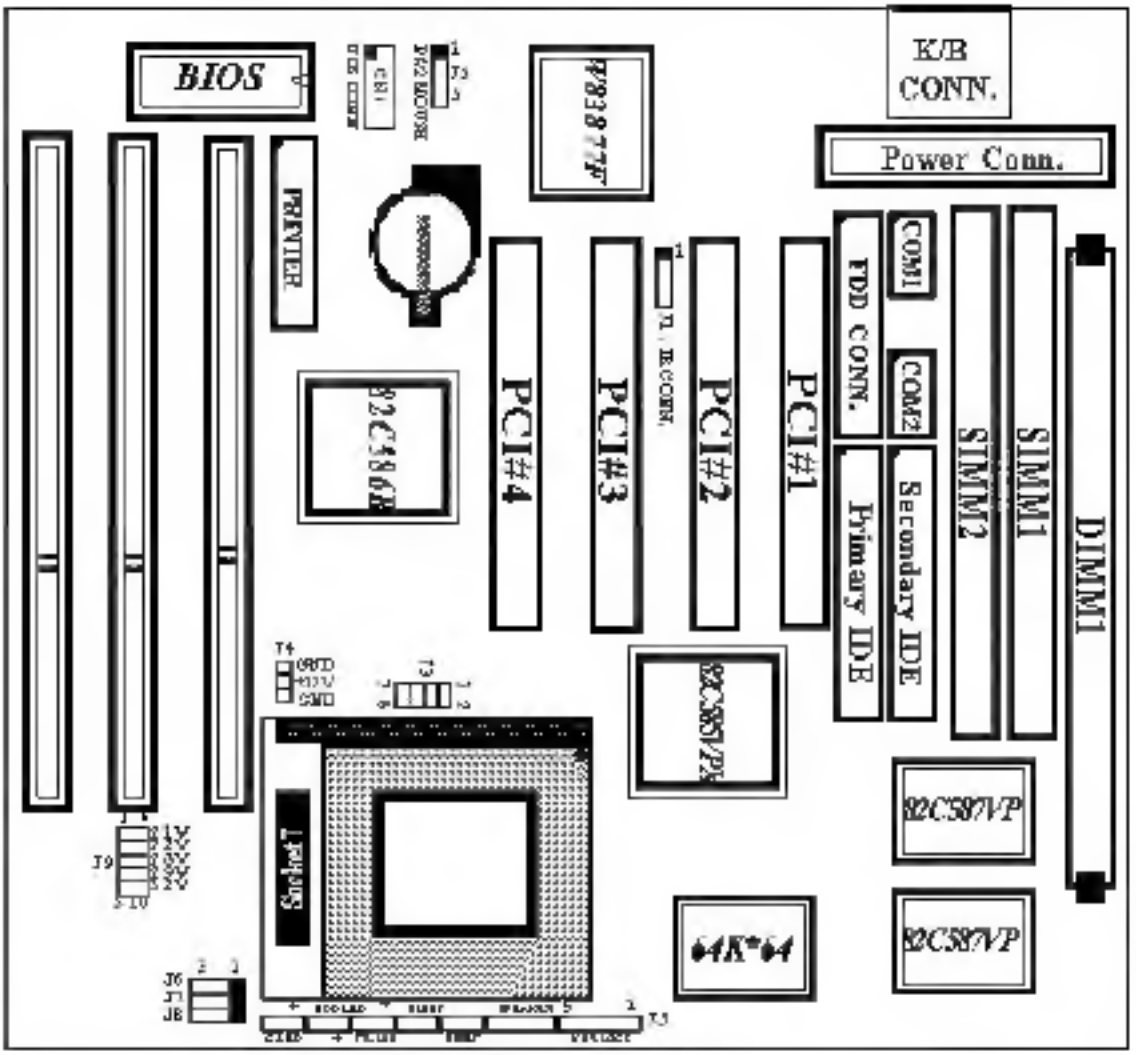

Figure 1-1

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Chapter 2
Hardware design

2-1 Mainboard Layout

The 5BVPXB is designed with VIA Apollo VPX/97 PCIset chipset which is developed by VIA Corporation to fully support Pentium Processor PCI/ISA system. The VIA Apollo VPX/97 PCIset chipset can increase integration and improve performance designs. The chipset provides an integrated IDE controller with two high performance IDE interfaces for up to four IDE devices (hard devices, CD-ROM device, etc). The Winbond W83877F Super I/O controller provides the standard PC I/O function: floppy interface, two 16 Byte FIFO serial ports and EPP/ECP capable parallel port. The **5BVPXB** layout is shown in the previous page for user's reference. **Care must be taken** when inserting memory modules, inserting CPU or even plugging PCI card into associated slots to avoid damaging any circuits or sockets on board. A cooling fan is strongly recommended when installing Pentium/Pentium MMX/K5/K6/6x86/6x86L/MX processor due to possible overheat.

The 5BVPXB supports a minimum of 8MB and a maximum of 192MB of System Memory while L2 Cache is 512KB synchronous SRAM Onboard to increase system performance. (Refer to **Page 2-6 Cache Memory Configuration** for the details)

The 5BVPXB supports standard Fast Page, EDO (Extended Data Out or Hyper Page Mode) or synchronous DRAM. **The 5BVPXB** provides two 72-pin SIMM and one 168-pin DIMM sites for memory expansion. The sockets support 1M x 32(4MB), 2M x 32(8MB), 4M x 32(16MB), and 8M x 32(32MB) single-sided or double-sided memory modules. The memory timing requires 70 ns Fast page devices or 60 ns EDO DRAM. (DRAM Modules may be parity [x 36] or non-parity [x 32])

The 5BVPXB supports **two Onboard PCI IDE** connectors, and automatically detects IDE harddisk type by BIOS utility automatic.

The 5BVPXB supports Award Plug & Play BIOS for the ISA and PCI cards. The BIOS can be located in Flash EPROM which can replace BIOS code easily if necessary.

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2-2 Connectors and Jumpers

This section describes all connectors and jumpers equipped in the mainboard. Please refer to **Figure 1-1** for location of each connector and jumper.

KeyLock - Keyboard lock switch & Power LED connector
1.Power LED(+)
2.N/C
3.GND
4.Keylock
5.GND

Speaker - connect to the system's speaker for beeping.
1 Speaker
2.N/C
3.GND
4 GND

Reset Switch - Closed to restart system.

Sleep/Resume switch - Closed to enter sleep mode. A keystrobe or mouse movement (mouse driver exists). Will instantly "wake up" the system.

Turbo LED indicator - LED ON when higher speed is selected.
There is no deturbo function so that the turbo LED is always ON

IDE LED indicator - LED ON when Onboard PCIIDE Harddisks activate.

Power Saving LED indicator - LED ON when system is in any Saving mode.

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J1 

IrDA/ASKIR CONNECTOR

1 VCC
2 NC
3 IRRX
4 GND
5 IRTX

J2 

PS/2 MOUSE CONNECTOR

1 RED wire
2 BLUE wire
3 GREEN wire
4 NC
5 YELLOW wire

J4 

The Power Supply (+12V) of the CPU Cooling FAN

1 GND
2 +12V
3 GND

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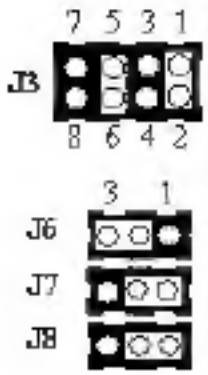

Intel Pentium® Processor / Pentium® MMX Processor / AMD K5 / K6 Installation				
Clock/CPU Op.	J3	J6	J7	J8
60/90 MHz	3-4, 5-6	1-2	1-2	1-2
66/100 MHz	1-2, 5-6			
60/120 MHz	3-4, 5-6	2-3	1-2	1-2
66/133 MHz	1-2, 5-6			
60/150 MHz	3-4, 5-6	2-3	2-3	1-2
66/166 MHz	1-2, 5-6			
66/200 MHz	1-2, 5-6	1-2	2-3	1-2
66/233 MHz	1-2, 5-6	1-2	1-2	1-2
@ 66/266 MHz	1-2, 5-6	2-3	1-2	2-3
@ 66/300 MHz	1-2, 5-6	2-3	2-3	2-3
@ 66/333 MHz	1-2, 5-6	1-2	2-3	2-3

Cyrix & IBM 6x86/6x86L/6x86MX Installation					
CPU	Clock Op.	J3	J6	J7	J8
6x86L-PR150+	60MHz * 2	3-4, 5-6	2-3	1-2	1-2
6x86L-PR166	66MHz * 2	1-2, 5-6			
6x86L-PR200+	75MHz * 2	3-4, 7-8			
6x86MX-PR166	66MHz * 2	1-2, 5-6	2-3	1-2	1-2
6x86MX-PR200	75MHz * 2	3-4, 7-8			
6x86MX-PR166	60MHz * 2.5	3-4, 5-6	2-3	2-3	1-2
6x86MX-PR200	66MHz * 2.5	1-2, 5-6			
6x86MX-PR233	75MHz * 2.5	3-4, 7-8			
@ 6x86MX-PR333	66MHz * 3	1-2, 5-6	1-2	2-3	1-2
@ 6x86MX-PR266	75MHz * 3	3-4, 7-8			
@ 6x86MX-PR266	66MHz * 3.5	1-2, 5-6	1-2	1-2	1-2

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	idt C6 Processor Installation					
	CPU	Clock Op.	J3	J6	J7	J8
	C6-DS120	60MHz * 2	3-4, 5-6	2-3	1-2	1-2
	C6-DS133	66MHz * 2	1-2, 5-6			
	C6-DS180	60MHz * 3	3-4, 5-6	1-2	2-3	1-2
	C6-DS200	66MHz * 3	1-2, 5-6			
@	C6-DS240	60MHz * 4	3-4, 5-6	2-3	1-2	2-3
@	C6-DS266	66MHz * 4	1-2, 5-6			
@	C6-DS300	60MHz * 5	3-4, 5-6	1-2	2-3	2-3
@	C6-DS333	66MHz * 5	1-2, 5-6			

@ These jumper settings are reserved for the future CPU versions. When the future CPU versions are ready and suitable for this mainboard, these jumper settings will be correctly updated.

J9 CPU Vcore voltage selection

1-6	2.1V Reserved
2-7	2.2V Reserved for AMD K6 in the future
3-8	2.8V For Intel Pentium MMX & Cyrix 6x86L
4-9	2.9V For AMD K6/PR2-166/200 & Cyrix 6x86MX
5-10	3.2V For AMD K6/PR2-233/266

Note : J9 is for Vcore Settings of dual voltage CPUs. Please ignore the settings of single voltage CPUs. Such as Intel Pentium Processor, AMD K5, Cyrix M1 and idt C6 here.

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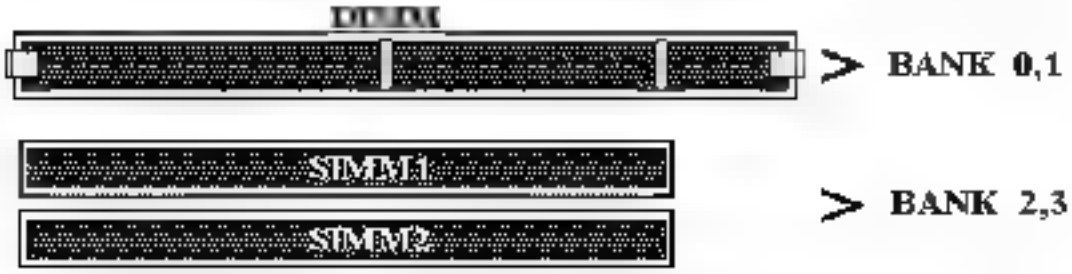
2 3 System Memory Configuration

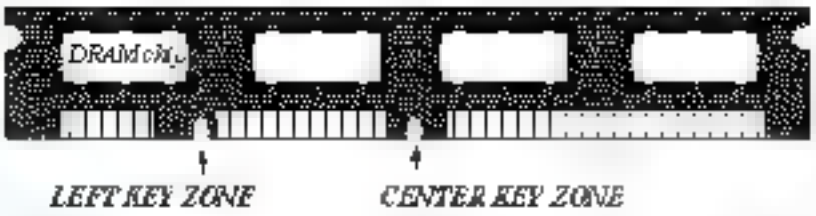
The 5BVPXB supports different type of settings for the system memory The following figures and table provides all possible memory combinations (Please refer to **Appendix C: Memory Configuration Table** for the details



DIMM1 BANK0	SIMM1,2 BANK1	TOTAL Memory
SDRAM	EDO/FPDRAM	MAX = 192MB
[16MB 32MB 64MB 128MB] x1	[4MB 8MB 16MB 32MB] x2	

NOTE 1. 5BVPXB supports both Fast Page DRAM and EDO DRAM SIMMs, but they cannot be used in the same memory bank

2. The KEY ZOOM of the DIMM socket is 3.3V Unbuffered



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2-4 Integrated PCI Bridge

The **5BVPXB** utilizes Apollo VPX97 PCIset chipset to support Intel Pentium processor PCI/ISA system. The VLA Apollo VPX97 PCIset chipset consists of the VT82C597VPX system controller (TSC), two 82C587VP Data Path (TDP) devices and the 82C586VP PCI-to-ISA bridge (PIB). It provides an interface which translates CPU cycle into PCI bus cycle, and PCI burst read/write capability. In addition, it provides high performance PCI arbitor to support four PCI Masters Rotating Priority Mechanism and Hidden Arbitration Scheme Minimize Arbitration Overhead.

There are four interrupt signals called INTA#, INTB#, INTC# and INTD#. The **5BVPXB** adapts the PCI auto-configuration with the system Plug and Play capability. When the system is turned on after adding or removing a PCI add-on card, the BIOS automatically configure interrupts, DMA channels, I/O space, and other parameters. You do not have to configure jumpers or worry about potential resource conflicts. Because PCI cards use the same interrupt resource as ISA cards, you must specify the interrupt used by ISA add-on cards in the BIOS Setup utility.

However, if a "Legacy card" such as plugging a paddle card and cable into an ISA slot or plugging in the system, modification in the **ROM SETUP UTILITY** becomes necessary. First of all, you must enter **PCI CONFIGURATION SETUP** utility in the **ROM SETUP UTILITY** main menu to set "Auto" for **PCI IDE IRQ MAP TO**.

Secondly, you must enter the **CHIPSET FEATURES SETUP UTILITY** in the **ROM SETUP UTILITY** main menu to set "Disabled" for the **Onboard Primary PCI IDE** and the **Onboard Secondary PCI IDE**. When you plug an ISA I/O card into the system, you should select "Enabled" for the **Onboard Primary and Secondary PCI IDE** from the **CHIPSET FEATURES SETUP UTILITY** too.

You can set the system interrupt request (IRQ) on some "Legacy cards" which have no paddle card and cable, refer to user's manual of the card, to a proper system IRQ even. In general, card's Primary is assigned to INTA and Secondary is assigned to INTB. If the card is plugged into slot 1, then slot 1's INTA and INTB are connected to PIRQ0 and PIRQ1. Because the 5BVPXB's INT may also route INT1 from the slot refer to Page 3-1 for interrupt mapping. Then you then enter the **PCI CONFIGURATION SETUP** option in the **ROM SETUP UTILITY** main menu and set the field of **PCI IDE IRQ MAP TO** that depends on which slot you have the legacy card plugged).

CHAPTER 3
AWARD BIOS SETUP

Award's ROM BIOS provides a built-in setup program which allows user to modify the basic system configuration and hardware parameters. The modified data will be stored in a battery-backed CMOS RAM so data will be retained even when the power is turned off. In general, the information saved in the CMOS RAM stays unchanged unless there is a configuration change in the system, such as a hard drive replacement or a new device installation.

If this does happen you will need to reconfigure your configuration parameter.

To Enter Setup Propgram

Power on the computer and press <Del> key immediately. This will bring you into BIOS CMOSSETUPUTILITY.

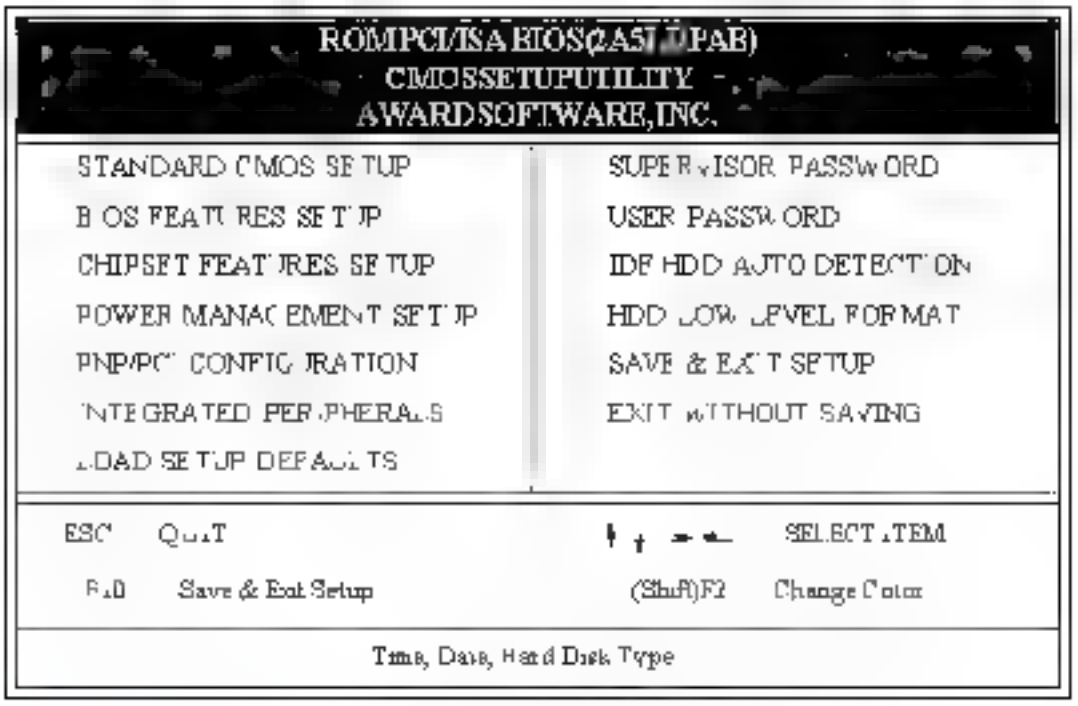

Figure 3-1 CMOS SETUP UTILITY

The menu displays all major selection items. Select the item you need to reconfigure. The selection is made by moving cursor (press any direction key) to the item and press the Enter key. An on-line help message is displayed at the bottom of the screen as the cursor is moving to various items which provides a better understanding of each function. When a selection is made, the menu of selected item will appear so the user can modify the associated configuration parameters.

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3-1 STANDARD CMOS SETUP

Choose "**STANDARD CMOS SETUP**" in the **CMOS SETUP UTILITY** Menu (Fig. 3-1). The **STANDARD CMOS SETUP** allows user to configure system setting such as the current date and time, type of hard disk drive installed, floppy drive type, and display type. Memory size is auto-detected by the BIOS and displayed for your reference. When a field is highlighted (use direction keys to move cursor and <Enter> key to select), the entries in the field will be changed by pressing <PgDn> or <PgUp> keys or user can enter new data directly from the keyboard.

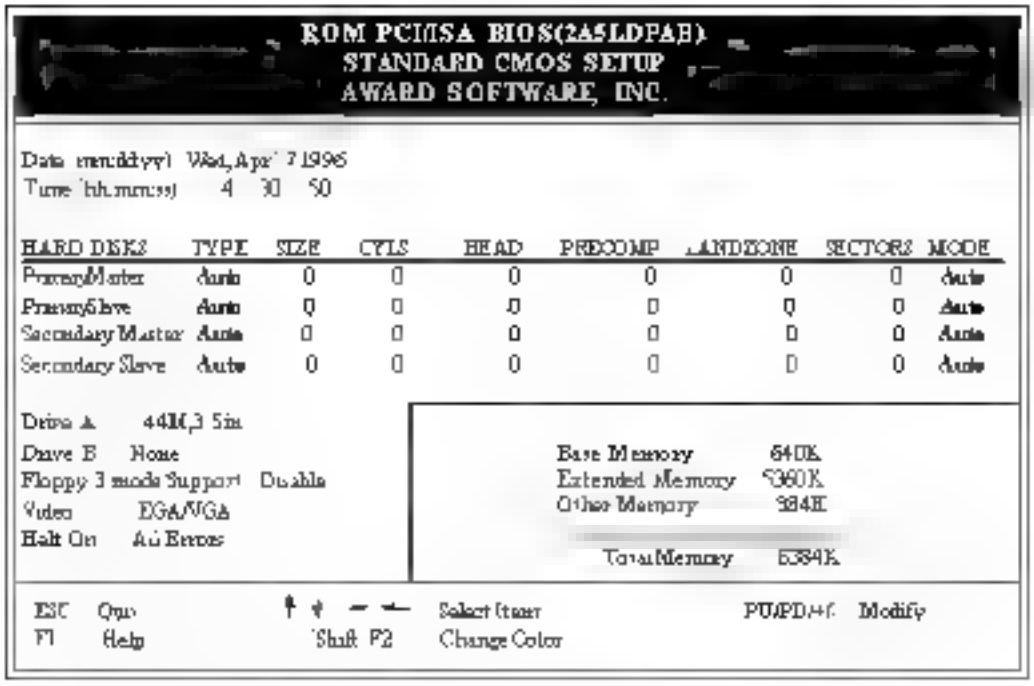

Figure 3-2 STANDARD CMOS SETUP

NOTE: If the hard disk Primary Master/Slave and the Secondary Master/Slave are set as "Auto", then the hard disk size and model will be auto-detected.

NOTE: The **'Halt On .'** field is to determine when to halt the system by the BIOS if an error occurs.

3-2 BIOS FEATURES SETUP

Selecting the "**BIOS FEATURES SETUP**" option in the **CMOS SETUP UTILITY** menu allows user to change system related parameters in the displayed menu. This menu shows all of the manufacturer's default values of the 5BVPXB. Again, user can move the cursor by pressing direction keys and <PgDn> or <PgUp> keys to modify the parameters. Pressing [F1] key to display help message of the selected item.

This setup program also provides 2 convenient ways to load the default parameter data from BIOS [F6] or CMOS [F7] area if shown data is corrupted. This provides the system a capability to recover from any possible error.

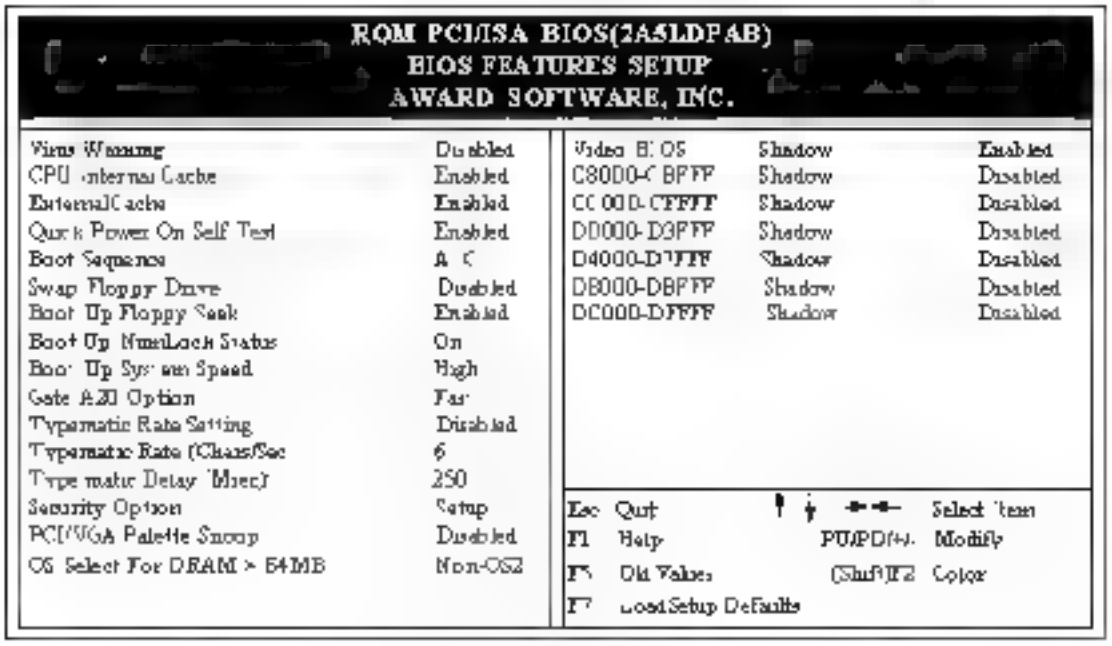

Figure 3-3 BIOS FEATURES SETUP

Note The **Security Option** contains **"setup"** and **"system"**. The **"setup"** indicates that the password setting is for CMOS only while the **"system"** indicates the password setting is for both CMOS and system boot up.

- **Virus Warning:** This category flashes on the screen. During and after the system boots up, any attempt to write to the boot sector or partition table of the hard disk drive will halt the system and an error message will appear. You should then run an anti-virus program to locate the virus. Keep in mind that this feature protects only the boot sector, not the entire hard drive. Default value is Disabled.

  Enabled Activates automatically when the system boots up causing a warning message to appear when any attempt to access the boot sector or hard disk partition table.

  Disabled No warning message to appear when any attempt to access the boot sector or hard disk partition table.

- **CPU Internal Cache External Cache** These two categories speed up memory access. However, it depends on CPU/chipset design. The default value is Enabled. If your CPU is without Internal Cache then this item "CPU Internal Cache" will not be shown.

  Enabled Enable cache

  Disable Disable cache

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- **Quick Power On Self Test** This category speeds up Power On Self Test (POST) after you power on the computer If it is set to Enable, BIOS will shorten or skip some checking items during POST
  Enabled Enable quick POST
  Disabled Normal POST

- **Boot Sequence**:This category determines which drive is searched first for the O S(Operating System The default value is A C
  A,C The system will search for floppy disk drive first then hard disk drive
  C,A The system will search for hard disk drive first then floppy disk drive

- **Swap Floppy Drive** This will swap your physical drive letters A&B if you are using two floppy disks The default value is Disabled
  Enabled Floppy A & B will be swapped under the O/S
  Disabled Floppy A & B will be not swapped

- **Boot Up Floppy Seek.** During Power-On-Self-Test (POST), BIOS will determine if the floppy disk drive installed is 40 or 80 tracks Only 360K type is 40 tracks while 720K 1 2M and 1 44M are all 80 tracks The default value is Enabled
  Enabled BIOS searches for floppy disk drive to determine if it is 40 or 80 tracks Note that BIOS cannot tell from 720K, 1 2M or 1 44M drive type as they are all 80 tracks
  Disabled BIOS will not search for the type of floppy disk drive by track number Note that there will not be any warning message if the drive installed is 360K

- **Boot Up NumLock Status**: The default value is On
  On Keypad is number keys
  Off Keypad is arrow keys

- **Boot UP System Speed**: Select default system speed The system will run at the selected speed after the system boots
  High Set the speed to high
  Low Set the speed to low

- **Gate A20 Option**: This refers to the way the system addresses memory above 1MB (extended memory) The default value is Fast
  Normal: The A20 signal is controlled by keyboard controller or chipset hardware
  Fast The A20 signal is controlled by Port 92 or chipset specific method

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- **Typematic Rate Setting** This determines the typematic rate
  Enabled Enable typematic rate and typematic delay programming.
  Disabled Disable typematic rate and typematic delay programming. The system BIOS will use default value of 2 items and the default is controlled by the keyboard.

- **Typematic Rate(Chars/Sec):**

6 6 characters per second	**8 8 characters per second.**
10 10 characters per second	**12: 12 characters per second**
15 15 characters per second	**20: 20 characters per second**
24 24 characters per second	**30: 30 characters per second**

- **Typematic Delay(Msec):** This determines the time between the first and second character displayed when holding a key
  250 250msec
  500 500 msec
  750 750 msec
  1000 1000 msec

- **Security Option:** This category allows you to limit access to the system and Setup, or just to Setup. The default value is Setup.
  System The system will not boot and the access to Setup will be denied if the correct password is not entered at the prompt.
  Setup The system will boot, but the access to Setup will be denied if the correct password is not entered at the prompt.

- **PCI/VGA Palette Snoop:** This filed controls the ability of a primary PCI VGA controller to share a common palette when a snoop write cycles, with an ISA video card. The default value is Disabled.
  Enabled: If an ISA card connects to a PCI VGA card via the VESA connector and the ISA card connects to VGA monitor and uses the RAMDAC of PCI card, the PCI/VGA Palette Snoop is enabled.
  Disabled: Disable the VGA card Palette snoop function.

- **Video BIOS Shadow:** It determines whether video BIOS will be copied to RAM, however, it is optional from chipset design. Video Shadow will increase the video speed.
  Enabled Video shadow is enabled.
  Disabled Video shadow is disabled.

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- C8000 CBFFF **Shadow**
  CC000 CFFFF **Shadow**
  D0000 D3FFF Shadow
  D4000 D7FFF Shadow
  D8000 DBFFF **Shadow**
  DC000 DFFFF **Shadow**

These categories determine whether optional ROM will be copied to RAM by 16K byte or 32K byte perunit and the size depends on the chipset

Enabled Optional shadow is enabled

Disabled Optional shadow is disabled

3.3 CHIPSET FEATURES SETUP

Choose the "CHIPSET FEATURES SETUP" in the CMOS SETUP UTILITY menu to display the following menu.

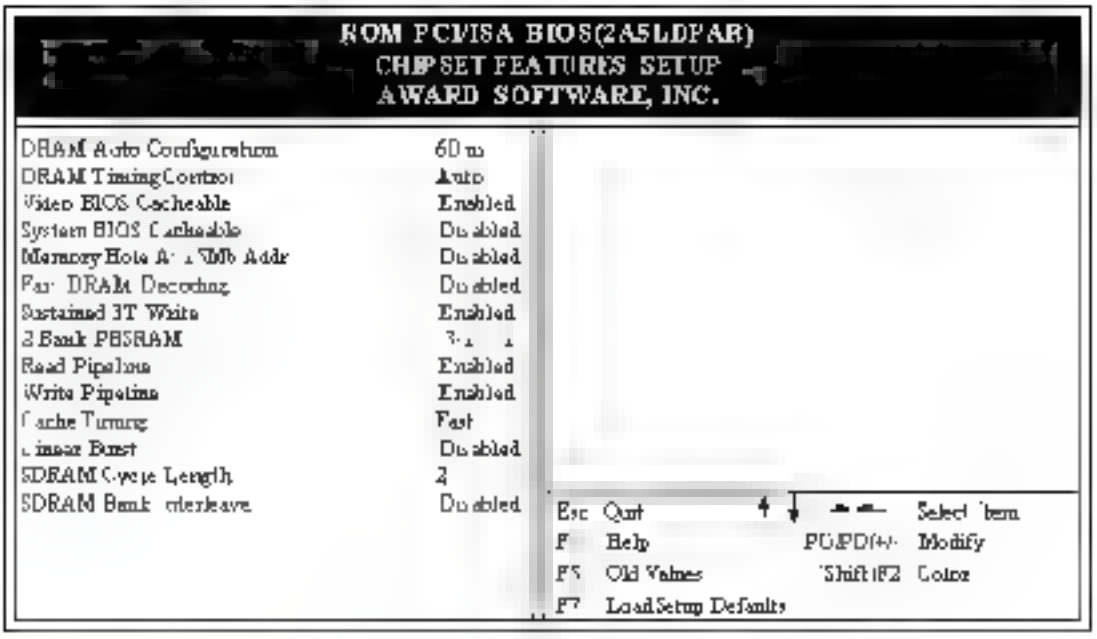

Figure 3-4 CHIPSET FEATURES SETUP

Note: When you insert slower memory modules in the system and set a faster timing, maybe the system will hang up

- **DRAM Timing.** The default value is 60ns
  60ns 2 faster Burst Wait State. for 60~70ns Fast Page Mode/EDO DRAM
  70ns 3 slower Burst Wait State for 70ns Fast Page Mode/EDO DRAM

- **Video BIOS Cacheable. The default value is Enabled**
  Enabled Enabled the Video BIOS Cacheable to speed up the VGA Performance
  Disabled Disabled the Video BIOS Cacheable function

- **Memory Hole at 15M-16M.** The default value is Disabled
  Disabled: Normal Setting
  Enabled This field enabeds the main memory 5~ 6MB remap to ISA BUS

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3-4 POWER MANAGEMENT SETUP

Choose the "POWER MANAGEMENT SETUP" in the CMOS SETUP UTILITY to display the following screen. This menu allows the user to modify the power management parameters and IRQ signals. In general, these parameters should not be changed unless it is absolutely necessary.

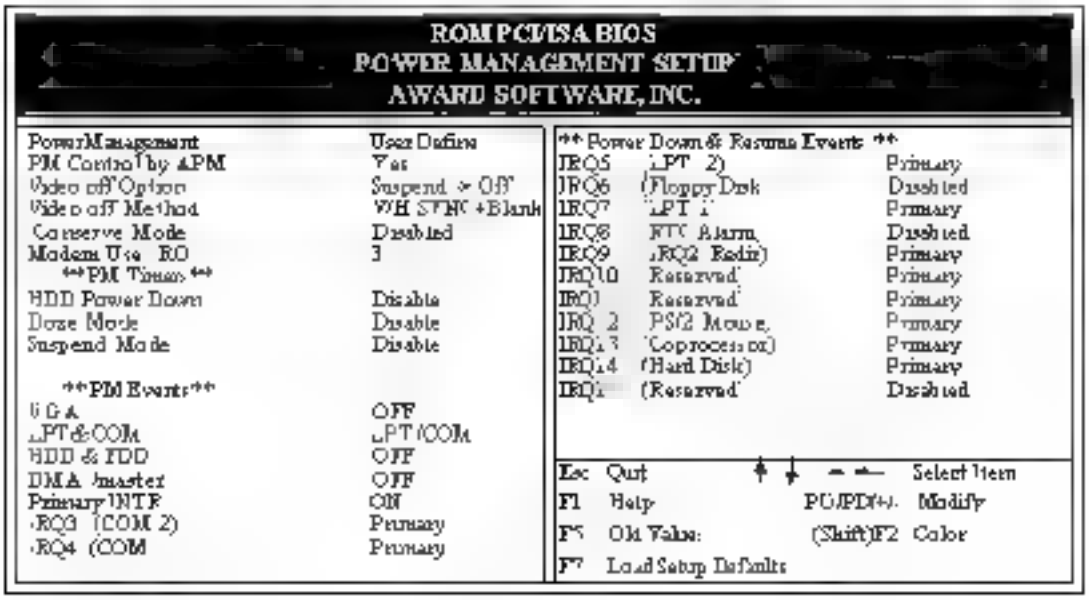

Figure 3-5 POWER MANAGEMENT SETUP

Again, user can move the cursor by pressing direction keys to the field needed to be modified and press <PgDn> or <PgUp> to alter item selection. You can only change the content of **Doze Mode**, **Standby Mode**, and **Suspend Mode** when the **Power Management** is set to **User Define**.

3-4-1 The Description of the Power Management

A. Power Management mode selection.

Disabled : The system operates in NORMAL conditions (Non GREEN) and the Power Management function is disabled.

Max saving: This mode will maximize the power saving capability.

Min saving: This mode will minimize the power saving capability.

User define: Allow user to define time out parameters to control power saving mode. Refer to item B shown below.

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PM Events.
AWARD BIOS defines 15 PM Events in the power management mode (Doze & suspend) The user can initialize any PM Events to be "Enable" or "Disable" When the system detects all of the enabled events do not have any activity It will start the system Doze timer first if the "Power Management" is not "Disabled" Once the system Doze timer is turned out it will process doze power saving procedure by starting the system suspend timer When the suspend timer turns out all of the CPU clock will stop by dropping system clock down to zero and remains this way until any one of the "Enabled" event occurs

3-5 PNP/PCI CONFIGURATION

The PNP/PCI configuration program is for the user to modify the PCI/ISA IRQ signals when various PCI/ISA cards are inserted in the PCI or ISA slots

WARNING Any improper setting IRQ could cause system can't pick out the resources

ROM PCI/ISA BIOS(2A5LDPAB)
PNP/PCI CONFIGURATION
AWARD SOFTWARE, INC.

PNP Installed		No	CPU to PCI Write Buffer	Enabled
Resources Controlled By		Manual	PCI Dynamic Bursting	Enabled
Reset Configuration Data		Disabled	PCI Master 0 WS Write	Enabled
			PCI Peer Concurrency	Enabled
IRQ-3	assigned to	Legacy ISA	PCI Delay Transaction	Disabled
IRQ-4	assigned to	Legacy ISA		
IRQ-5	assigned to	PCI/ISA PnP	PCI IRQ Actived By	Level
IRQ-7	assigned to	Legacy ISA	PCI IDE IRQ Map To	PCI-AUTO
IRQ-9	assigned to	PCI/ISA PnP	Primary IDE INT#	A
IRQ-10	assigned to	PCI/ISA PnP	Secondary IDE INT#	B
IRQ-11	assigned to	PCI/ISA PnP		
IRQ-12	assigned to	PCI/ISA PnP		
IRQ-14	assigned to	Legacy ISA		
IRQ-15	assigned to	Legacy ISA		
DMA-0	assigned to	PCI/ISA PnP		
DMA-1	assigned to	PCI/ISA PnP		
DMA-3	assigned to	PCI/ISA PnP		
DMA-5	assigned to	PCI/ISA PnP		
DMA-6	assigned to	PCI/ISA PnP		
DMA-7	assigned to	PCI/ISA PnP		

ESC	Quit	↑ ↓ → ←	Select Item
F1	Help	PU/PD/+/-	Modify
F5	Old Value	(Shift) F2	Color
F7	Load Setup Defaults		

Figure 3-6 PCI CONFIGURATION SETUP

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- **Resource Controlled By:** The default value is Manual
  Manual: The field defines that the PNP Card's resource is controlled by manual. You can set whether IRQ-X or DMA X is assigned to PCI/ISA PNP or Legacy ISA Cards.
  Auto: If your ISA card and PCI card are all PNP cards. Set this field Auto. The BIOS will assign the interrupt resource automatically.

- **Reset Configuration Data:** The default value is Disabled.
  Disabled: Normal Setting.
  Enabled: If you plug some Legacy cards in the system and record into ESCD (Extended System Configuration Data). You can set this field to be Enabled and to clear ESCD at one time, when some Legacy cards are removed.

- **PCI IDE IRQ Map To:** The default value is PCI AUTO.

  When you have true PCI cards plugged into the system, you will not need to change any thing here in the **SETUP** program. However if you do not know whether you are using a true PCI card, please refer to your PCI card user's manual for the details.

  When you have a Legacy card (described in section 2-5) to plug into the system a proper setting is extremely important or it may cause the system hung up. The diagram shown below tells you how the Rotating Priority Mechanism is designed.

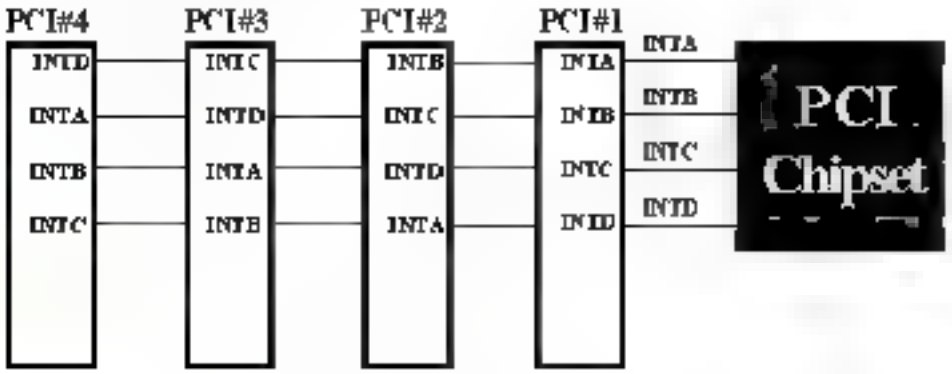

Figure 3-7 The Combination of PCI INT# Lines

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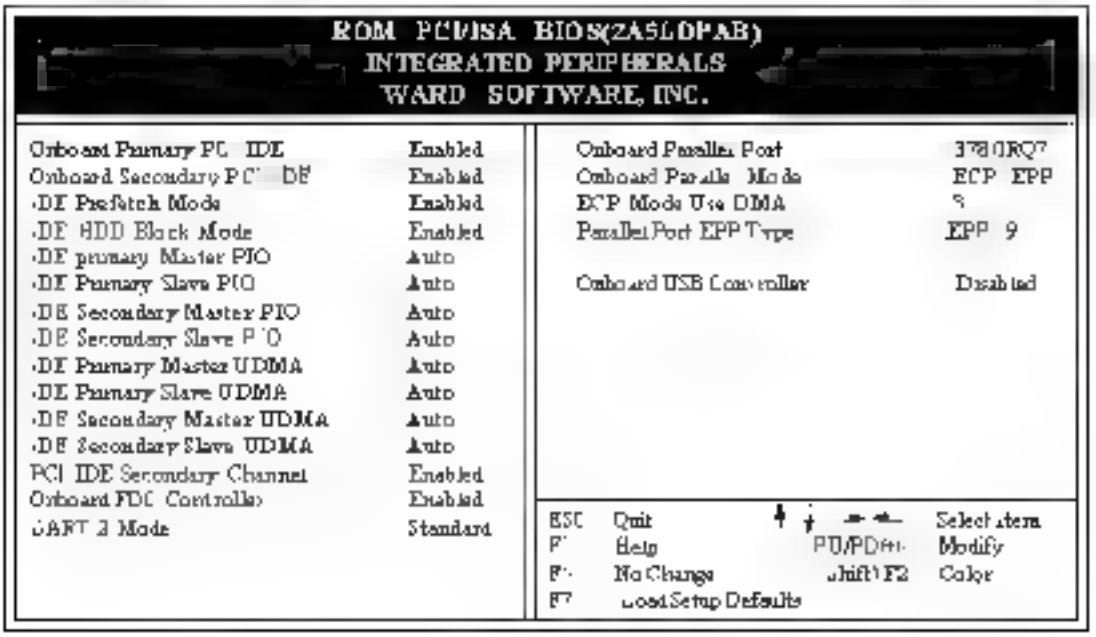
3-6 INTEGRATED PERIPHERALS



Note: If you don't use the Onboard IDE connector then use On-card (PCI or ISA card) IDE connector You have to set Onboard Primary PCI IDE. Disabled and Onboard Secondary PCI IDE Disabled from CHIPSET FEATURES SETUP UTILITY
The Onboard PCI IDE cable should be equal to or less than 18 inches (45 cm.).

- **IDE HDD Block Mode** The default value is Enabled.
  Enabled Enabled IDE HDD Block Mode The HDD transfer rate is better than Disable
  Disabled Disable IDE HDD Block Mode

- **PCI Slot IDE 2nd Channel** The default value is Enabled
  Enabled Enable secondary IDE port and BIOS will assign IRQ15 for this port
  Disabled Disable secondary IDE port and IRQ15 is available for other device

- **Onboard Primary PCI IDE.** The default value is Enabled.
  Enabled Enable Onboard 1st channel IDE port
  Disabled Disable Onboard 1st channel IDE port When use On-card (PCI or ISA card) IDE connector

- **Onboard Secondary PCI IDE** The default value is Enabled
  Enabled Enable Onboard 2nd channel IDE port
  Disabled Disable Onboard 2nd channel IDE port When use On-card (PCI or ISA card) IDE connector

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- **IDE Primary Master PIO** The default value is Auto
  Auto BIOS will automatically detect the Onboard Primary Master PCI IDE HDD Accessing mode
  Mode0~4 : Manually set the IDE Accessing mode

- **IDE Primary Slave PIO** The default value is Auto
  Auto BIOS will automatically detect the Onboard Primary Slave PCI IDE HDD Accessing mode
  Mode0~4 : Manually set the IDE Accessing mode

- **IDE Secondary Master PIO**: The default value is Auto
  Auto BIOS will automatically detect the Onboard Secondary Master PCI IDE HDD Accessing mode
  Mode0~4 : Manually set the IDE Accessing mode

- **IDE Secondary Slave PIO**: The default value is Auto
  Auto BIOS will automatically detect the Onboard Secondary Slave PCI IDE HDD Accessing mode
  Mode0~4 : Manually set the IDE Accessing mode

- **Onboard FDC Controller** The default value is Enabled.
  Enabled Enable the Onboard floppy drive interface controller
  Disabled Disable the Onboard floppy drive interface controller When using On-card ISA FDC's controller

- **Onboard UART 1** This field allows the user to select the serial port. The default value is 3F8H/IRQ4
  COM1: Enable Onboard Serial port 1 and address is 3F8H/IRQ4
  COM2: Enable Onboard Serial port 1 and address is 2F8H/IRQ3
  COM3: Enable Onboard Serial port 1 and address is 3E8H/IRQ4
  COM4: Enable Onboard Serial port 1 and address is 2E8H/IRQ3
  Disabled: Disable Onboard SMC CHIP's Serial port

- **Onboard UART 2** This field allows the user to select the serial port. The default value is 2F8H/IRQ3
  COM1: Enable Onboard Serial port 2 and address is 3F8H/IRQ4
  COM2: Enable Onboard Serial port 2 and address is 2F8H/IRQ3
  COM3: Enable Onboard Serial port 2 and address is 3E8H/IRQ4
  COM4: Enable Onboard Serial port 2 and address is 2E8H/IRQ3
  Disabled: Disable Onboard SMC CHIP's Serial port 2

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- **Onboard UART 2 Mode**: The default value is standard. This field allows the User to select the COM2 port that can support a serial Infrared Interface.
  Standard : Support a Serial Infrared Interface IrDA.
  HPSIR : Support a HP Serial Infrared Interface format.
  ASKIR: Support a Sharp Serial Infrared Interface format.

- **Onboard Parallel port**: This field allows the user to select the LPT port. The default value is 378H/IRQ7.
  378H : Enable Onboard LPT port and address is 378H and IRQ7.
  278H : Enable Onboard LPT port and address is 278H and IRQ5.
  3BCH : Enable Onboard LPT port and address is 3BCH and IRQ7.
  Disabled : Disable Onboard SMC CHIP's LPT port.

NOTE: **Parallel Port address is 378H/3BCH that selects the rounting of IRQ7 for LPT1**
Parallel Port address is 278H that selects the rounting of IRQ5 for LPT1

- **Parallel port Mode**: This field allows the user to select the parallel port mode. The default value is ECP+EPP.
  Normal : Standard mode IBM PC/AT Compatible bidirectional parallel port.
  EPP : Enhanced Parallel Port mode.
  ECP : Extended Capability Port mode.
  EPP+ECP : ECP Mode & EPP Mode.

ECP Mode USE DMA: This field allows the user to select DMA-1 or DMA-3 for the ECP mode. The default value is DMA-3.
DMA1 : The filed selects the rounting of DMA-1 for the ECP mode.
DMA3 : The filed selects the rounting of DMA-3 for the ECP mode.

3-7 LOAD SETUP DEFAULTS

The **'LOAD SETUP DEFAULTS'** function loads the system default data directly from ROM and initializes the associated hardware properly. This function will be necessary only when the system CMOS data is corrupted.

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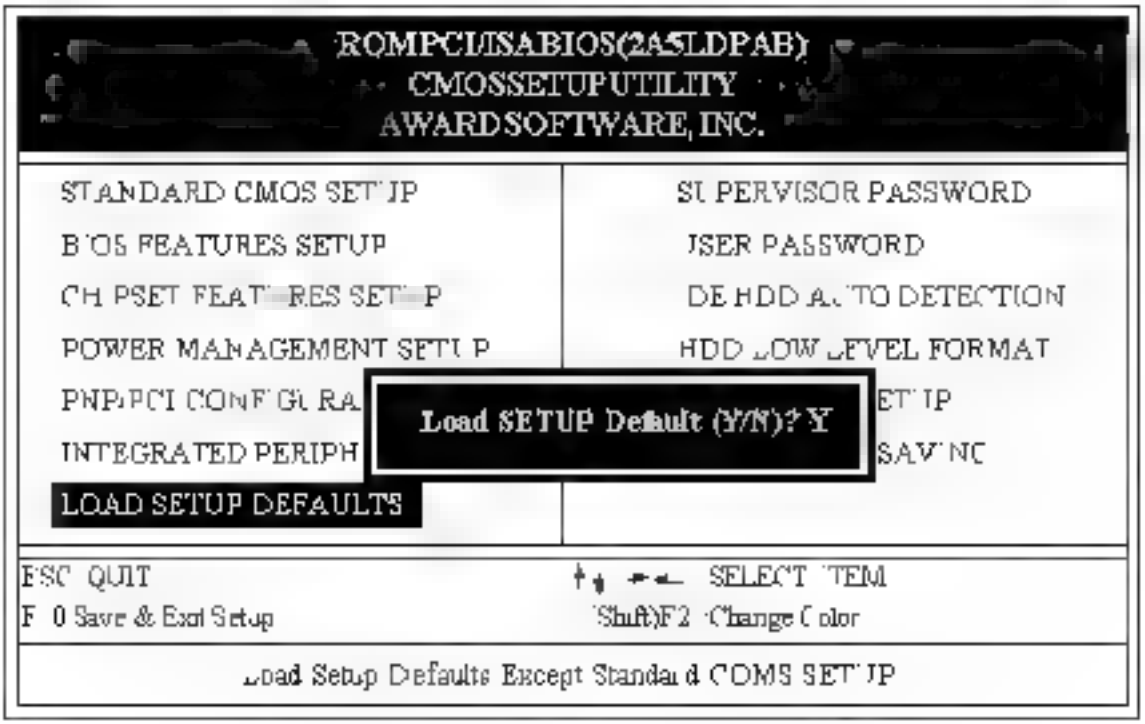

Figure 3-8 LOAD SETUP DEFAULT

3-8 CHANGE SUPERVISOR or USER PASSWORD

To change the password, choose the **'SUPERVISOR PASSWORD or USER PASSWORD'** option from the **CMOS SETUP UTILITY** menu and press [Enter].

NOTE Either **'Setup'** or **"System"** must be selected in the **'Security Option'** of the **BIOS FEATURES SETUP** menu. (Refer to Figure 3-3 for the details)

If CMOS is corrupted or the option is not used, a default password stored in the ROM will be used. The screen will display the following message:

Enter Password:

Press the Enter key to continue after proper password is given.

2. If CMOS is corrupted or the option was used earlier and the user wish to change default password, the **SETUP UTILITY** will display a message and ask for a confirmation.

Confirm Password:

3. After pressing the Enter key (ROM password if the option was not used) or current password (user defined password), the user can change the password and store new one in CMOS RAM. A maximum of 8 characters can be entered.

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3.9 IDE HDD AUTO DETECTION

The "IDE HDD AUTO DETECTION" utility is a very useful tool especially when you do not know which kind of hard disk type you are using. You can use this utility to detect the correct disk type installed in the system automatically. **But now** you can set **HARD DISK TYPE** to **Auto** in the **STANDARD CMOS SETUP**. You do not need the "IDE HDD AUTO DETECTION" utility. The BIOS will Auto-detect the hard disk size and mode on display during POST.

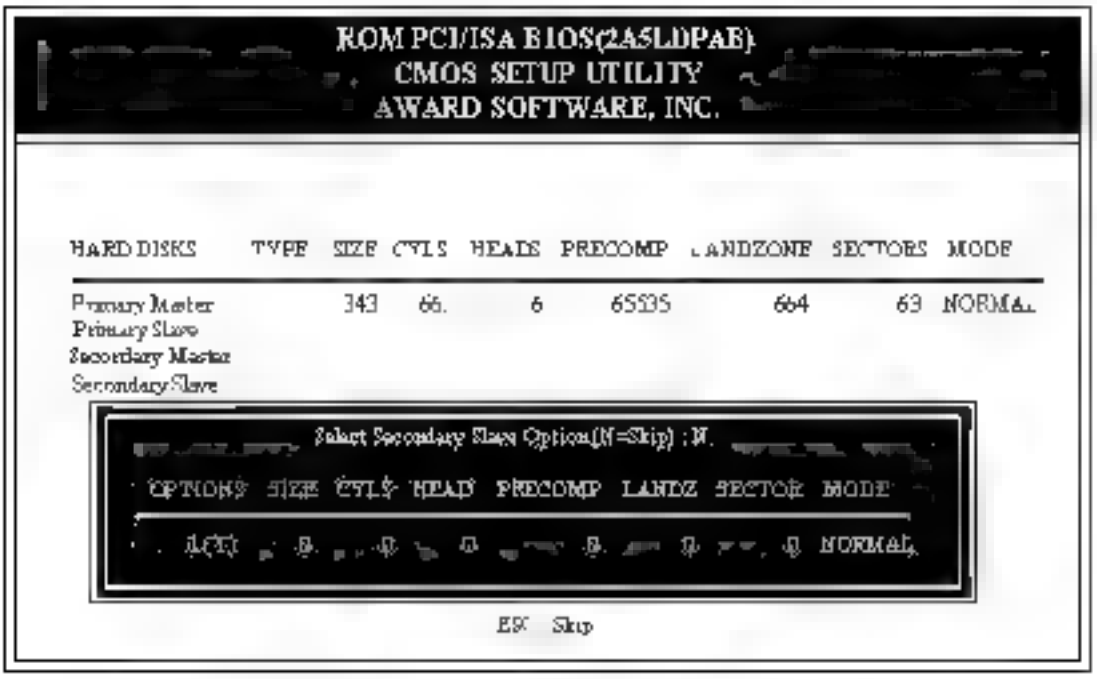

Figure 3-9 IDE HDD AUTO DETECTION

NOTE: HDD Modes

The Award BIOS supports 3 HDD modes: NORMAL, LBA and LARGE.

NORMAL mode

Generic access mode that is neither the BIOS nor the IDE controller will make transformations during accessing.

The maximum numbers of cylinders, head & sectors for NORMAL mode are 1024, 16 and 63.

	no. Cylinder	1024
x	no. Head	16
x	no. Sector	63
÷	no. per sector	512
		528 Megabytes

If user sets his HDD to NORMAL mode, the maximum accessible HDD size will be 528 Megabytes even though its physical size may be greater than that.

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Note

To support LBA or LARGE mode of HDDs there must be some softwares involved. All softwares are located in the Award HDD Service Routine (INT 13h). It may fail to access a HDD with LBA (LARGE) mode selected if you are running under an Operating System which replaces the whole INT 13h. UNIX operating systems do not support either LBA or LARGE and must utilize the Standard mode. UNIX can support drives larger than 528MB.

3-10 HDD LOW LEVEL FORMAT

Interleave

Select the interleave number of the hard disk drive that you wish to perform a low level format on. You may select from 1 to 8. Check the documentation that came with the drive for the correct interleave number or select 0 for automatic detection.

Auto scan bad track

This allows the utility to scan first then format by each track.

Start

Press< Y >to start low level format.

3-11 SAVE & EXIT SETUP

The **'SAVE & EXIT SETUP"** option will bring you back to boot up procedure with all the changes you just recorded in the CMOS RAM.

3-12 EXIT WITHOUT SAVING

The **'EXIT WITHOUT SAVING'** option will bring you back to normal boot up procedure without saving any data into CMOS RAM. All old data in the CMOS will not be destroyed.

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Chapter 4
Technical Information

4-1 I/O & MEMORY MAP

MEMORY MAP

Address Range	Size	Description
[00000-7FFFF]	512K	Conventional memory
[80000-9FBFF]	127K	Extended Conventional memory
[9FC00-9FFFF]	1K	Extended BIOS data area if PS/2 mouse is installed
[A0000-C7FFF]	160K	Available for Hi DOS memory
[C8000-DFFFF]	96K	Available for Hi DOS memory and adapter ROMs
[E0000-EFFFF]	60K	Available for UMB
[F0000-F3FFF]	4K	Video service routine for Monochrome & CGA adaptor
[F4000-F7FFF]	32K	BIOS CMOS setup utility
[F8000-FCFFF]	20K	BIOS runtime service routine (2)
[FD000-FDFFF]	4K	Plug and Play ESCD data area
[FE000-FFFFF]	8K	BIOS runtime service routine (1)

I/O MAP

[000-01F]	DMA controller (Master)
[020-021]	INTERRUPT CONTROLLER (Master)
[022-023]	CHIPSET control registers I/O ports
[040-05F]	TIMER control registers
[060-06F]	KEYBOARD interface controller 8042
[070-07F]	RTC ports & CMOS I/O ports
[080-09F]	DMA register
[0A0-0BF]	INTERRUPT controller (Slave)
[0C0-0DF]	DMA controller (Slave)
[0F0-0FF]	MATH COPROCESSOR
[1F0-1F8]	HARD DISK controller
[278-27F]	PARALLEL port 2
[2B0-2DF]	GRAPHICS adapter controller
[2F8-2FF]	SERIAL port 2
[360-36F]	NETWORK ports
[378-37F]	PARALLEL port
[3B0-3BF]	MONOCHROME & PARALLEL port adapter
[3C0-3CF]	EGA adapter
[3D0-3DF]	CGA adapter
[3F0-3F7]	FLOPPY DISK controller
[3F8-3FF]	SERIAL port 1

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4-2 TIME & DMA CHANNELS MAP

TIME MAP	TIMER Channel 0	System timer interrupt
	TIMER Channel 1	DRAM REFRESH request
	TIMER Channel 2	SPEAKER tone generator
DMA CHANNELS	DMA Channel 0	Available
	DMA Channel 1	Onboard ECP Option
	DMA Channel 2	FLOPPY DISK (SMC CHIP)
	DMA Channel 3	Onboard ECP default
	DMA Channel 4	Cascade for DMA controller 1
	DMA Channel 5	Available
	DMA Channel 6	Available
	DMA Channel 7	Available

4-3 INTERRUPT MAP

NMI :		Parity check error
IRQ (H/W) .	0	System TIMER interrupt from TIMER 0
	1	KEYBOARD output buffer full
	2	Cascade for IRQ 8- 5
	3	SERIAL port 2
	4	SERIAL port 1
	5	PARALLEL port 2
	6	FLOPPY DISK (SMC CHIP)
	7	PARALLEL port 1
	8	RTC clock
	9	Available
	0	Available
		Available
	2	PS/2 Mouse
	3	MATH coprocessor
	4	Onboard HARD DISK (IDE1 channel
	5	Onboard HARD DISK (IDE2 channel

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4.4 RTC & CMOS RAM MAP

RTC & CMOS	00	Seconds
	01	Second alarm
	02	Minutes
	03	Minutes alarm
	04	Hours
	05	Hours alarm
	06	Day of week
	07	Day of month
	08	Month
	09	Year
	0A	Status register A
	0B	Status register B
	0C	Status register C
	0D	Status register D
	0E	Diagnostic status byte
	0F	Shutdown byte
	10	FLOPPY DISK drive type byte
	11	Reserve
	12	HARD DISK type byte
	13	Reserve
	14	Equipment type
	15	Base memory low byte
	16	Base memory high byte
	17	Extension memory low byte
	18	Extension memory high byte
	19- 2d	
	2E- 2F	
	30	Reserved for extension memory low byte
	31	Reserved for extension memory high byte
	32	DATE CENTURY byte
	33	INFORMATION FLAG
	34- 3F	Reserve
	40- 7F	Reserved for CHIPSET SETTING DATA

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APPENDIX A: POST CODES

ISA POST codes are typically output to port address 80h.

POST(hex)	DESCRIPTION
[illegible]	Reserved.
C0	Turn off OEM specific cache, shadow
03	1. Initialize EISA registers (EISA B/O only) 2. Initialize all the standard devices with default values. Standard devices includes: -DMA controller (8237) -Programmable Interrupt Controller (8259) -Programmable Interval Timer (8254) -RTC chip
04	Reserved.
05	1. Keyboard Controller Self Test. 2. Enable Keyboard Interface.
06	Reserved.
07	Verifies CMOS's basic R/W functionality.
C1	Auto-detection of onboard DRAM & Cache.
C5	Copy the B/O S from ROM into E0000-FFFFF shadow RAM so that POST will go faster.
08	Test the first 256K DRAM.
09	OEM specific cache initialization (if needed).
[illegible]	1. Initialize the first 32 interrupt vectors with corresponding interrupt handlers. Initialize INT no. from 33-120 with Dummy (Suprious) Interrupt Handler. 2. Issue CPUID instruction to identify CPU type. 3. Early Power Management initialization. (OEM specific)
0E	1. Verify the RTC time is valid or not. 2. Detect bad battery. 3. Read CMOS data into BIOS stack area. 4. PnP initializations including: (PnP B/O S only) Assign CSN to PnP ISA card. Create resource map from ESCD. 5. Assign I/O & Memory for PCI devices. (PCI B/O S only)

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POST(hex)	DESCRIPTION
0C	nitialization of the BIOS Data Area (40:00 - 40:FF)
0D	1. Program some of the Chipset's value according to Setup "Early Setup value" Program 2. Measure CPU speed for display & decide the system clock speed. 3. Video initialization including Monochrome / CGA / EGA/VGA. If no display device found, the speaker will beep
0E	1. Test video RAM. (If Monochrome display device found) 2. Show messages including: Award Logo / Copyright string, BIOS Data code & Part No OEM specific sign on messages Energy Star Logo (Green BIOS ONLY) CPU brand, type & speed Test system BIOS checksum. (Non-Compress Version only
0F	DMA channel 0 test
10	DMA channel test
11	DMA page registers test
12-13	Reserved
14	Test 8254 Timer 0 Counter 2
15	Test 8259 interrupt mask bits for channel
16	Test 8259 interrupt mask bits for channel 2
17	Reserved
19	Test 8259 functionality
1A-1D	Reserved
1E	If EISA NVM checksum is good, execute EISA initialization (EISA BIOS only)
1F-29	Reserved
30	Detect Base Memory & Extended Memory Size
31	1. Test Base Memory from 256K to 640K 2. Test Extended Memory from 1M to the top of memory

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POST(hex)	DESCRIPTION
32	1.Display the Award Plug & Play BIOS Extension message (PnP BIOS only) 2.Program all onboard super I/O chips (if any) including COM ports, LPT ports, FDD port . . according to setup value
33-3B	Reserved
3C	Set flag to allow users to enter CMOS Setup Utility.
3D	1.Initialize Keyboard. 2.Install PS2 mouse.
3E	Try to turn on Level 2 cache. Note : Some chipset may need to turn on the L2 cache in this stage. But usually, the cache is turn on later in POST 61h.
3F-40	Reserved
BF	1.Program the rest of the Chipset's value according to Setup. (Later Setup Value Program) 2.If auto-configuration is enabled, programmed the chipset with pre-defined Values
41	Initialize floppy disk drive controller
42	Initialize Hard drive controller.
43	If it is a PnP BIOS, initialize serial & parallel ports
44	Reserved.
45	Initialize math coprocessor
46-4D	Reserved.
4E	If there is any error detected (such as video, kb...), show all the error messages on the screen & wait for user to press <F1> key.
4F	1.If password is needed, ask for password 2.Clear the Energy Star Logo [Green BIOS only]
50	Write all CMOS values currently in the BIOS stack area back into the CMOS
51	Reserved.

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POST (hex) DESCRIPTION

52 1.Initialize all ISA ROMs.
2.Later PCI initializations. (PCI BIOS only)
-assign IRQ to PCI devices.
-initialize all PCI ROMs
3.PnP initializations. (PnP BIOS only)
-assign IO, Memory, IRQ & DMA to PnP ISA devices.
-initialize all PnP ISA ROMs
4.Program shadows RAM according to Setup settings.
5.Program parity according to Setup setting.
6.Power Management Initialization.
-Enable/Disable global PM.
-APM interface initialization.

53 1.If it is NOT a PnP BIOS, initialize serial & parallel ports.
2.Initialize time value in BIOS data area by translate the RTC time value into a timer tick value.

60 Setup Virus Protection. (Boot Sector Protection) functionality according to Setup setting.

61 1.Try to turn on Level 2 cache.
Note : if L2 cache is already turned on in POST 3D, this part will be skipped.
2.Set the boot up speed according to Setup setting.
3.Last chance for Chipset initialization.
4.Last chance for Power Management initialization. (Green BIOS only)
5.Show the system configuration table

62 1.Setup daylight saving according to Setup value.
2.Program the NUM Lock, typematic rate & typematic speed according to Setup setting.

63 1.If there is any changes in the hardware configuration, update the ESCD information. (PnP BIOS only)
2.Clear memory that have been used.
3.Boot system via INT 19H.

FF System Booting. This means that the BIOS already pass the control right to the operating system.

Unexpected Errors;

POST (hex) DESCRIPTION

B0 If interrupt occurs in protected mode.

B1 Unclaimed NMI occurs.

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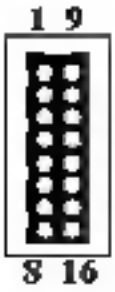
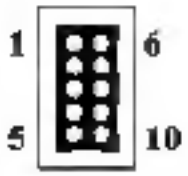
APPENDIX B: I/O CONNECTORS

CN6 : USB CONNECTOR:



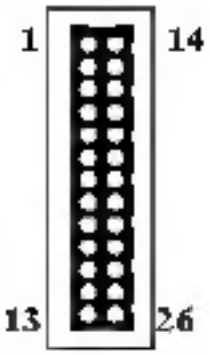
Signal Name	Pin	Pin	Signal Name
USB_VCC	1	9	Ground
USB_data0-	2	10	Ground
USB_data0+	3	11	Ground
Ground	4	12	Ground
USB_VCC	5	13	Ground
USB_data1-	6	14	Ground
USB_data1+	7	25	Ground
Ground	8	26	Ground

CN1/COM1,CN2/COM2 : Serial Ports Connector



Signal Name	Pin	Pin	Signal Name
DCD	1	6	DSR
SIN	2	7	RTS
SOUT	3	8	CTS
DTR	4	9	RI
GND	5	10	N.C.

CN7 : Parallel Port Connector



Signal Name	Pin	Pin	Signal Name
STROBE-	1	14	AUTO FEED-
Data Bit 0	2	15	ERROR-
Data Bit 1	3	16	INIT-
Data Bit 2	4	17	SLCT IN-
Data Bit 3	5	18	Ground
Data Bit 4	6	19	Ground
Data Bit 5	7	20	Ground
Data Bit 6	8	21	Ground
Data Bit 7	9	22	Ground
ACJ-	10	23	Ground
BUSY	11	24	Ground
PE	12	25	Ground
SLCT	13	26	N.C.

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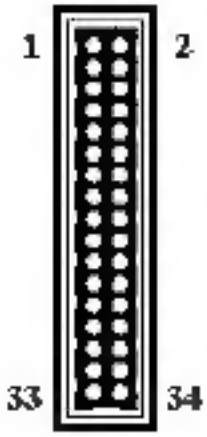
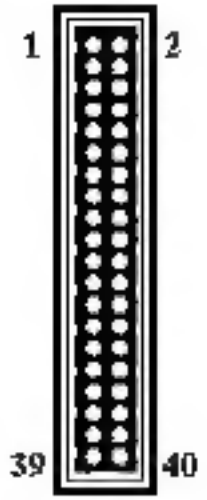
CN3 : Floppy Disk Connector



Signal Name	Pin	Pin	Signal Name
Ground	1	2	FDHDIN
Ground	3	4	Reserved
Ground	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable
Ground	11	12	Drive Select B-
Ground	13	14	Drive Select A-
Ground	15	16	Motor Enable
Ground	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data
Ground	23	24	Write Gate
Ground	25	26	Track 00-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	SIDE 1 SELECT-
Ground	33	34	Diskette

CN4/CN5 : Primary, Secondray IDE Connector



Signal Name	Pin	Pin	Signal Name
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DRQ3	21	22	Ground
I/O Write-	23	24	Ground
I/O Read-	25	26	Ground
IOCHRDY	27	28	BALE
DACK3-	29	30	Ground
IRQ14	31	32	IOCS16-
Addr 1	33	34	Ground
Addr 0	35	32	Addr 2
Chip Select 0-	37	38	Chip Select 1-
Activity	39	40	Ground

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